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Patentanmeldung Nr. Patent application No. Demande de brevet n°

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

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Transceiver with multi-state direct digital synthesizer driven phase locked loop

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Transceiver with multi-state Direct Digital Synthesizer driven Phase Locked Loop

The invention relates to a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer driven phase locked loop.

The invention also relates to a digital synthesizer driven phase locked loop for use in a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising said digital synthesizer driven phase locked loop, and to a phase locked loop for use in a digital synthesizer driven phase locked loop for use in a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising said digital synthesizer driven phase locked loop, and to a digital synthesizer for use in a digital synthesizer driven phase locked loop for use in a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising said digital synthesizer driven phase locked loop, and to a system comprising at least one portable unit and at least one network unit for radio communication, with at least one unit comprising at least one transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer driven phase locked loop, and to a portable unit comprising a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer driven phase locked loop, and to a network unit comprising at least one transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer driven phase locked loop, and to a method for transmitting signals in a transmitting mode and for receiving signals in a receiving mode via a digital synthesizer driven phase locked loop.

Such a transceiver is for example used in time division duplex (TDD) telecommunication systems or time division multiple access (TDMA) telecommunication systems, with said portable unit for example being a mobile phone and with said network unit for example being a base station or a router or a server etc.

performance allowing the generation of an improved modulated signal, with said PLL comprising, in said oscillating state, a second filtering performance allowing demodulation with reduced phase noise.

A fourth embodiment of the transceiver according to the invention as defined in claim 5 is advantageous in that said first filter for example being a loop filter and said second filter for example being a narrow band filter are being selected via a low cost switch. The first control signal and the second control signal respectively may be completely different control signals or may be the same control signal having a first value and a second value respectively.

A fifth embodiment of the transceiver according to the invention as defined in claim 6 is advantageous in that said PLL generates, dependently upon the state in which it is, a modulated signal destined for a transmitter part or a non-modulated signal destined for a non-transmitter part.

A sixth embodiment of the transceiver according to the invention as defined in claim 7 is advantageous in that low cost switches are used for supplying said modulated signal via said transmitter part to said antenna and for supplying said non-modulated signal to a demodulator for demodulating a radio signal received via said antenna and said receiver part. The transmitter part for example comprises an auto gain controller, a filter and a power amplifier. The receiver part for example comprises a filter, a low noise amplifier and an auto gain controller, with said demodulator for example working in a Zero Intermediate Frequency mode or a Near Zero Intermediate Frequency mode. The first control signal and the second control signal respectively may be completely different control signals or may be the same control signal having a first value and a second value respectively. Said demodulator and/or said receiver part together form said non-transmitter part.

Embodiments, of the digital synthesizer driven phase locked loop according to the invention, of the phase locked loop according to the invention, of the digital synthesizer according to the invention, of the system according to the invention, of the portable unit according to the invention, of the network unit according to the invention, and of the method according to the invention, correspond with the embodiments of the transceiver according to the invention.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments(s) described hereinafter.

signal generator 45. An output of modulation signal generator 45 is coupled to a first input of switch 32, and an output of non-modulation signal generator 44 is coupled to a second input of switch 32. An output of control signal generator 43 is coupled to control inputs of switches 11, 32, 3 and 5.

In time division telecommunication systems like time division duplex (TDD) telecommunication systems or time division multiple access (TDMA) telecommunication systems, during one or more first time slots, modulated signals are transmitted from the transceiver according to the invention to an other transceiver (transmitting mode), and during one or more second time slots, modulated signals are sent from the other transceiver to the transceiver according to the invention (receiving mode). According to prior art, a DDS driven PLL is used for generating a reference signal, like in US 5,859,570, which discloses a DDS driven PLL operating in a frequency synthesizing mode.

According to the invention - based upon a basic idea, inter alia, of using important parts in low cost transceivers, having a transmitting mode and a receiving mode, for both modes, instead of using different parts for different modes - said DDS driven PLL, in said transmitting mode, is in a modulating state, with said DDS driven PLL, in said receiving mode, being in an oscillating state.

Thereto, mode detector 41 detects the transceiver, during a first time-interval, being in a transmitting mode, for example via a coupling not shown to transmitter part 2, and/or for example by making a calculation, with said first and second time slots being standardized, and informs processor/memory system 42, which instructs modulation signal generator 45 to generate a modulation signal (for example in response to an audio signal originating from a man-machine-interface not shown and coupled to processor/memory 42) and instructs control signal generator 43 to generate a first control signal. In response to this first control signal, switch 32 supplies said modulation signal originating from modulation signal generator 45 to DDS 24, and switch 11 couples first filter 12 to VCO 10, with first filter 12 for example being a loop filter for improving the PLL function and for example having a bandwidth which is equal to or a little larger than the (occupied) bandwidth of the modulation signal. DDS 24 receives a multiplied clock signal comprising clock pulses via multiplier 31 and clock generator 30, and receives said modulation signal. At the hand of DDS 24, any signal including complex waveforms can be generated by defining one or more of at least three parameters being frequency, phase and amplitude respectively. These three parameters respectively can be controlled by frequency control words (with frequency modulation being achieved before/in phase accumulator 23), phase control words (with phase

control signal or a further control signal originating from controller 40, connecting VCO 10 with demodulator 6. Receiver part 4, for example comprising a filter, a low noise amplifier and an auto gain controller, receives a (modulated) radio signal via antenna 1 and switch 3. Switch 3, for example in response to said second control signal or a further control signal originating from controller 40 via a coupling not shown, connects antenna 1 with receiver part 4, and supplies a gain controlled, amplified and filtered (modulated) radio signal to demodulator 6, which demodulates (for example via a Zero IF mode or Near Zero IF mode, which is very advantageous in that no expensive and bulky SAW IF filters are required) said last mentioned signal via said locked non-modulated reference signal. As a result, a demodulated signal is supplied to controller 40, for example via processor/memory system 42 to a man-machine-interface not shown which in response generates an audio signal. So, during this second time-interval, the transceiver is in a receiving mode, and the DDS driven PLL 24,10-15 is in an oscillating state.

By letting a transmitter part and a non-transmitter part (comprising a receiver part and/or a demodulator) of said transceiver according to the invention share a single DDS driven PLL, which in said transmitting mode, is in a modulating state, and which in said receiving mode, is in an oscillating state (a frequency synthesizer state), a low cost transceiver has been provided. Compared to prior art, like US 5,859,570 disclosing a DDS driven PLL always being in a frequency synthesizer state, the transceiver according to the invention is very advantageous, due to using said DDS driven PLL for different purposes. In other words, the transceiver is implemented using Radio Frequency direct modulation based on the DDS driven PLL and Radio Frequency demodulation (for example Zero IF, or Near Zero IF) based on the DDS driven PLL, which makes the transceiver low cost and small in size.

The invention solves the problem, inter alia, of providing a low cost transceiver (due to said transmitter part and said non-transmitter part - comprising said receiver part and/or said demodulator - sharing a single DDS driven PLL), which has a simple construction (by using one or more of said low cost switches) and nevertheless offers a good performance (due to the PLL dependently upon its mode using a specific mode-dependent filter). As a result, the transceiver according to the invention has a fast locking time in combination with less components, and therefore can have a smaller size and a lower weight.

Each block shown or not shown, can be 100% hardware, 100% software or a mixture of both. Each block shown or not shown can be integrated with each other block

CLAIMS:

1. Transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer (24) driven phase locked loop (10-15), characterized in that said digital synthesizer driven phase locked loop (24,10-15), in said transmitting mode, is in a modulating state, with said digital synthesizer driven phase locked loop (24,10-15), in said receiving mode, being in an oscillating state.

2. Transceiver according to claim 1, characterized in that said digital synthesizer driven phase locked loop (24,10-15) receives, in said modulating state, a modulation signal, with said digital synthesizer driven phase locked loop (24,10-15), in said oscillating state, receiving a non-modulation signal.

3. Transceiver according to claim 2, characterized in that said transceiver comprises a controller (40) for generating said modulation signal and for generating control signals, with a switch (32) being coupled to said controller (40) and said digital synthesizer driven phase locked loop (24,10-15) for in response to a first control signal supplying said modulation signal from said controller (40) to said digital synthesizer driven phase locked loop (24,10-15) and in response to a second control signal supplying said non-modulation signal to said digital synthesizer driven phase locked loop (24,10-15).

4. Transceiver according to claim 1 or 2, characterized in that said digital synthesizer driven phase locked loop (24,10-15) comprises, in said modulating state, a first filtering performance, with said digital synthesizer driven phase locked loop (24,10-15) comprising, in said oscillating state, a second filtering performance different from said first filtering performance.

5. Transceiver according to claim 4, characterized in that said digital synthesizer driven phase locked loop (24,10-15) comprises a first filter (12) for said first filtering performance and a second filter (13) for said second filtering performance, with a switch (11)

receiving signals in a receiving mode and comprising said digital synthesizer driven phase locked loop (24,10-15), characterized in that said digital synthesizer (24), in said transmitting mode, is in a modulating state, with said digital synthesizer (24), in said receiving mode, being in an oscillating state.

11. System comprising at least one portable unit and at least one network unit for radio communication, with at least one unit comprising at least one transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer driven phase locked loop (24,10-15), characterized in that said digital synthesizer driven phase locked loop (24,10-15), in said transmitting mode, is in a modulating state, with said digital synthesizer driven phase locked loop (24,10-15), in said receiving mode, being in an oscillating state.

12. Portable unit comprising a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer driven phase locked loop (24,10-15), characterized in that said digital synthesizer driven phase locked loop (24,10-15), in said transmitting mode, is in a modulating state, with said digital synthesizer driven phase locked loop (24,10-15), in said receiving mode, being in an oscillating state.

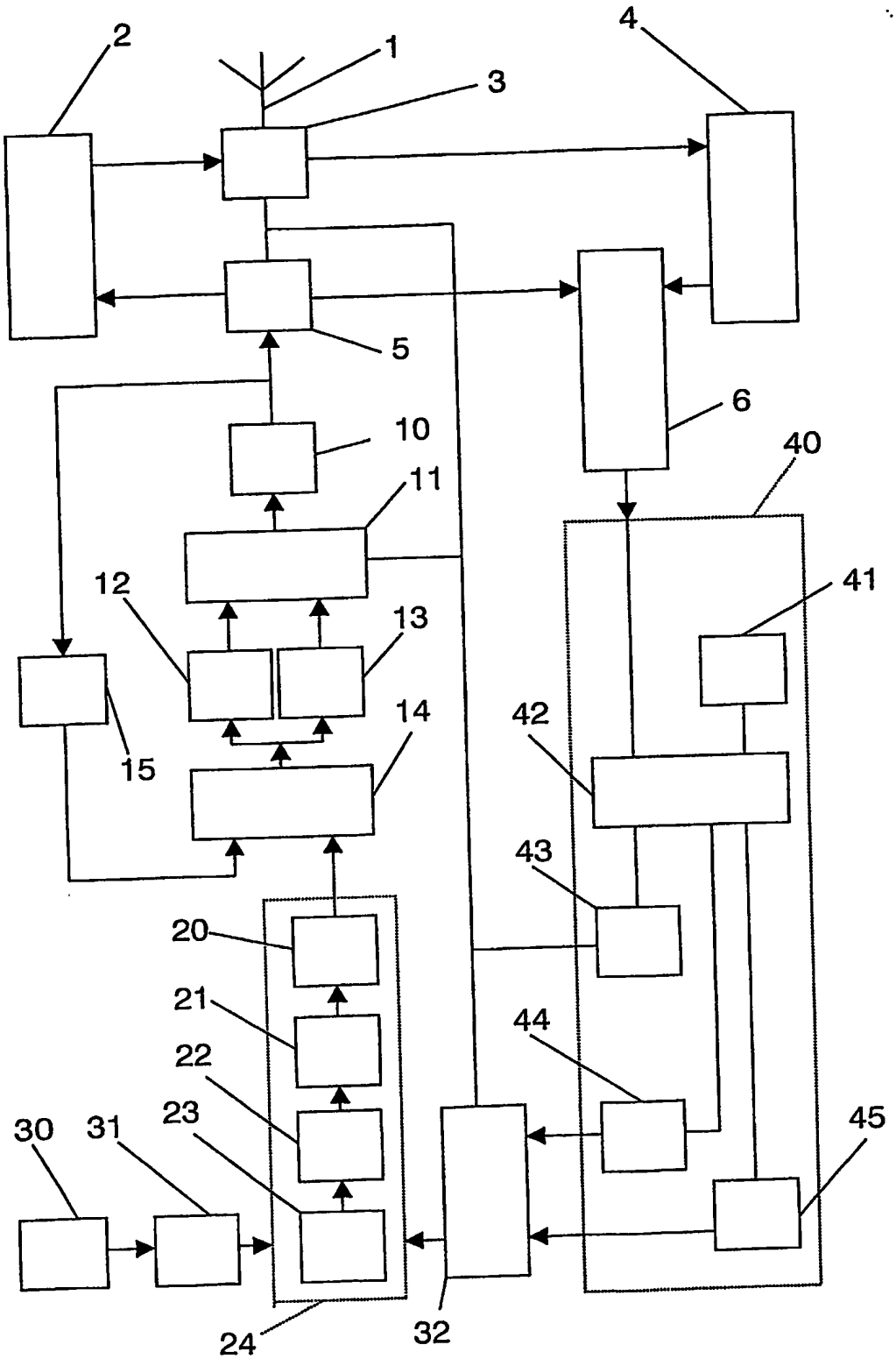
13. Network unit comprising at least one transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer driven phase locked loop (24,10-15), characterized in that said digital synthesizer driven phase locked loop (24,10-15), in said transmitting mode, is in a modulating state, with said digital synthesizer driven phase locked loop (24,10-15), in said receiving mode, being in an oscillating state.

14. Method for transmitting signals in a transmitting mode and for receiving signals in a receiving mode via a digital synthesizer driven phase locked loop (24,10-15), characterized in that said method comprises a first step of bringing said digital synthesizer driven phase locked loop (24,10-15), in said transmitting mode, in a modulating state, and a second step of bringing said digital synthesizer driven phase locked loop (24,10-15), in said receiving mode, in an oscillating state.

ABSTRACT:

Transceivers for use in time division telecommunication units like mobile phones and base stations can be produced at lower costs by, in a transmitting mode, switching the direct digital synthesizer (DDS 24) driven phase locked loop (PLL 10-15) into a modulating state and supplying a modulation signal to the DDS and switching in the PLL a first filter (12) allowing the generation of an improved modulated signal, and by, in a receiving mode, switching the DDS driven PLL into an oscillating state and supplying a non-modulation signal to the DDS and switching in the PLL a second filter (13) allowing demodulation with reduced phase noise. A transmitter part (2) and a non-transmitter part (4,6) share a single DDS driven PLL, based upon the basic idea of using important parts in low cost transceivers for both modes, instead of using different parts for different modes, and achieve a good performance.

Sole Fig.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